**Chip 8 Instruction Scheduling and Frequency**

If you search around for the processor speed of the Chip 8 you’re likely to find either no mention or the magic number 500Hz.

The reason for this is that Chip 8 is an interpreted language, similar to Python or Java (though far less complex) and as such the speed is dependent on the hardware it runs on, and the virtual machine running it.

If you don’t want that then 500-600hz is a great compromise between playability and shouldn’t cause any problems with code running, however if you do want to create an accurate emulator then it’s not going to be singular neat number. It will be dependent on which instruction is run on that cycle, as well and the instructions parameters and outputs.

Below is a table of all relevant instructions with the timing details and information about discrepancies. This information is compiled from [Laurence Scotford’s](http://laurencescotford.co.uk/) excellent [breakdown of the original Cosmac VIP Chip 8 virtual machine](http://laurencescotford.co.uk/?p=405).

|  |  |  |  |
| --- | --- | --- | --- |
| **Opcode** | **Average Time (µs)** | **Variance (±µs)** | **Notes** |
| **00E0** | 109 | 0 |  |
| **00EE** | 105 | 5 | Lower if page boundary not crossed Upper if page boundary is crossed |
| **1NNN** | 105 | 5 |
| **2NNN** | 105 | 5 |
| **3XNN** | 55 | 9 | Lower bound if true Upper bound if false |
| **4XNN** | 55 | 9 |
| **5XY0** | 73 | 9 |
| **6XNN** | 27 | 0 |  |
| **7XNN** | 45 | 0 |  |
| **8XY0** | 200 | 0 |  |
| **8XY1** | 200 | 0 |  |
| **8XY2** | 200 | 0 |  |
| **8XY3** | 200 | 0 |  |
| **8XY4** | 200 | 0 |  |
| **8XY5** | 200 | 0 |  |
| **8XY6** | 200 | 0 |  |
| **8XY7** | 200 | 0 |  |
| **8XYE** | 200 | 0 |  |
| **9XY0** | 73 | 9 | Lower bound if true Upper bound if false |
| **ANNN** | 55 | 0 |  |
| **BNNN** | 105 | 5 | Lower if page boundary not crossed Upper if page boundary is crossed |
| **CXNN** | 164 | 0 |  |
| **DXYN** | 22734 | 4634 | The time discrepancy is huge for this instruction due to it having so many contributing factors. This discrepancy also includes a 2355 to 3666 cycle delay while waiting for a screen draw to start. |
| **EX9E** | 73 | 9 | Lower bound if true Upper bound if false |
| **EXA1** | 73 | 9 |
| **FX07** | 45 | 0 |  |
| **FX0A** | 0 | 0 |  |
| **FX15** | 45 | 0 |  |
| **FX18** | 45 | 0 |  |
| **FX1E** | 86 | 14 | Lower if page boundary not crossed Upper if page boundary is crossed |
| **FX29** | 91 | 0 |  |
| **FX33** | 927 | 545 | Broken down into: 364µs (Base time) + \sum{digits} \* 73µs |
| **FX55** | 605 | 477 | Broken down into: 64µs (Base time) + X (Amount of registers) \* 64 µs |
| **FX65** | 605 | 477 |